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RICHTEK TECHNOLOGY CORP.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICHTEK TECHNOLOGY CORPORATION,

Plaintiff

v.

uPI SEMICONDUCTOR CORPORATION, SAPPHIRE TECHNOLOGY LIMITED, POWERCHIP TECHNOLOGY CORP., MAXCHIP ELECTRONICS CORP., SILICON XTAL CORPORATION, AMANDA DAI, JACKY LEE, MING CHEN, XYZ COMPANIES 1-4, and JOHN DOES 1-10,

Defendants.

Case No. 3:09-cv -05659-WHA

DECLARATION OF MARK HORENSTEIN, Ph.D., IN SUPPORT OF PLAINTIFF RICHTEK'S OPPOSITION TO DEFENDANTS' MOTION FOR STAY PENDING REEXAMINATION

I. INTRODUCTION

1. I have been retained by Richtek Technology Corporation ("Richtek") as an expert witness in this lawsuit. In this Declaration, I am providing my opinions regarding the validity of claims 1-11 and 26-27 of U.S. Patent No. 7,315,190 ("190 patent"). Specifically, I have been asked to address the non-final office dated December 17, 2010 submitted by the U.S. Patent & Trademark Office ("PTO") during reexamination of the 190 and the two Intersil datasheets relied upon by the Examiner as it pertains to validity issues in this lawsuit. I am not involved in any way with the prosecution of the 190 patent at the PTO, nor have I been asked to provide any assistance in prosecuting the 190 patent under reexamination. Based on my review of the Intersil datasheets and the Examiner's non-final office action, it is my opinion the two Intersil datasheets do not constitute invalidating prior art or raise any issues impinging on the validity of claims 1-11 and 26-27 of the 190 patent.

II. BACKGROUND AND QUALIFICATIONS

2. I am an expert in the area of integrated circuit (IC) design, structure, and operation. I received my B.S. Degree in Electrical Engineering from the Massachusetts Institute of Technology (MIT) in 1973, M.S. Degree in Electrical Engineering from University of California Berkeley (Berkeley) in 1975, and Ph.D. Degree in Electrical Engineering from MIT in 1978. I am a tenured Professor at Boston University (BU) in the Department of Electrical and Computer Engineering. I have taught and conducted research at BU for over thirty years since 1979. I have received five U.S. Patents, authored two text books used for teaching Electrical Engineering, and authored or co-authored a number of articles published in technical journals. I have also provided technical expertise in the fields of design and analysis of electrical and electronic IC circuits, power supplies, electromagnetic fields, and the issues surrounding the design of consumer products. The details of my education, work experience, fields of expertise, and qualifications are set forth in my *Curicula Vitae* ("CV") attached as **Exhibit A**.

III. SCOPE OF WORK

3. In reaching the opinions in this Declaration, I have reviewed the following:

- U.S. Patent No. 7,315,190 (RTK00000001-16) attached as **Exhibit B**;
- The prosecution history of the 190 patent and cited references;
- Non-Final Office Action ("NOA") dated December 17, 2010 for Reexamination Application No. 90/011,180 and is attached as **Exhibit C**;
- Intersil ISL6545, ISL6545A Datasheet Dated April 29, 2010 provided in the NOA and is attached as **Exhibit D**. I note that this Datasheet is not dated October 2005 as alleged by the Examiner in the NOA. I have searched for an October 2005 dated ISL6545 Datasheet and unable to obtain it.
- Intersil ISL6520 Datasheet dated March 2003 and is attached as **Exhibit E**;
- Intersil ISL6545A, ISL6545 Datasheet Dated November 15, 2006 publicly available over the Internet attached as **Exhibit F**.
- Intersil Press Release, "Intersil's PWM Controllers Integrate MOSFET Drivers and Eliminate the Need for a Current-Sensing Resistor," dated November 22, 2006 attached as **Exhibit G**.
- Other materials, documents, and information referenced in this Rebuttal Expert Report.

IV. TECHNOLOGY BACKGROUND

4. The 190 patent (RTK00000001-16) relates to a general class of integrated circuits (ICs) referred to as *switching power supplies*, which include DC-DC converters, controllers, and regulators. Such devices convert one voltage level to another and are essential components for electronic and computing devices. Such converters ensure that devices function properly, and they prevent damage that would otherwise occur due to excessive power overload. I will now provide background information on the technology at issue for these DC-DC converters, controllers, and regulators ("simply converters"). This background information will be useful in understanding the 190 patent.

A. Switching Power Supplies

5. Switching power supplies are a subset of circuits referred to broadly as "power supplies." Most electronic devices in use today, such as radios, cell phones, laptops, and desktop computers, require a source of voltage that one can, in principle, obtain from ordinary batteries. Most individuals are familiar with common batteries such as the AA, AAA, C, D, 9-V types, as they are regularly available in convenience stores, supermarkets, etc. By the nature of their internal chemistry, batteries provide a voltage of constant polarity and magnitude, usually referred to as direct-current (DC) voltage. A well-known problem with batteries is that they do not retain their energy. Rather, they discharge after some time and must be replaced or recharged. Thus, numerous versions of the above mentioned electronic appliances, if destined for continuous use, rely on power supplies in lieu of batteries to provide continuous power. Power for these boards is typically derived from power supplies connected to electrical outlets that provide voltage in AC form (e.g., 120 volts at 60 Hz in North and South America; 240 at 50 Hz volts in Europe and China, 100 volts in Japan).

6. The polarity of the line voltage supplied to residential and commercial buildings varies periodically in time, alternating sinusoidally between positive and negative polarities at regular intervals. In North and South America, for example, this change in polarity occurs 60 times per second (60 Hz), while in most other countries the frequency is 50 Hz. Voltages of such alternating polarity are commonly referred to as alternating-current (AC) voltages. Sometimes, AC line voltage is referred to simply as the "wall" voltage, referring to the power available at a common electrical wall outlet. It can thus be appreciated that the role of many power supplies is to transform AC line voltage into a source of DC voltage that can be used in lieu of common batteries. Such power supplies are sometimes called battery eliminators, power adaptors, wall cubes, AC adaptors, plug supplies, AC-to-DC converters, or (erroneously) "transformers."

7. For many years, the only power supplies available fell into the category of *linear* supplies. These circuits were formed from, typically, AC transformers, diodes, capacitors, resistors, and perhaps some transistors or voltage regulators under continuous operation. While

reliable, linear supplies were not the most efficient, and were relatively costly. With the appearance on the market of high-power transistors such as the power BJT (bipolar junction transistor) and vertical-channel MOSFET (metal-oxide-semiconductor field-effect transistor), alternative design approaches based on the *switching power supply* (SPS) technique emerged. Unlike the power elements in a linear supply, which operate continuously, the power transistors in an SPS operate as non-linear switches whose states are changed between "on" and "off" at high frequency. One advantage of switching power-supply technology is that low-cost power supplies can be designed that are much more efficient and compact than are more costly linear supplies delivering the same amount of power. Nowadays, almost all power supplies found on the market are of the switching variety.

8. Switching power supplies came into widespread use in the early to mid-1980's, and much attention was devoted by university and industry researchers to their further refinement and optimization. One consequence of these joint efforts was the emergence of various integrated circuits that contained, inside one tiny "chip" device, most all of the critical electrical elements needed to construct a switching supply.

B. PWM DC-TO-DC Converters or Controllers

9. Another class of power supply converts a DC voltage of one magnitude to a second DC voltage of a different magnitude. Such a supply is commonly referred to as a "voltage converter." Pulse-width modulation, explained below in more detail, is often used as a control method, hence these types of circuits are sometimes referred to as PWM DC-to-DC Converters and Controllers. In industry, the terms "controller", "converter", and "regulator" are often used interchangeably, and, as is my understanding, this fact has been confirmed by at least AMD and uPI witnesses. These controllers are often found in electronic and computing devices where they may, e.g., provide power to central processing units (CPUs) and graphical processing units (GPUs) (e.g., Intel CPUs and AMD's Radeon GPUs), graphics cards, and other elements found inside the computer. While the primary power source feeding a DC-DC converter is usually derived from an AC-to-DC converter, this is not always the case, as a DC-DC converter can also be powered directly from a battery.

10. One popular category of integrated circuit, and the subject of the ’190 patent is designed to implement DC-DC conversion via pulse-width modulation. Many pulse-width modulation power-supply circuits utilize the so-called “totem pole” driving configuration shown in the prior-art **FIG. 1** of the 190 patent reproduced below. (190 Patent at RTK00000003). As shown on the figure, this configuration makes use of two MOSFET switches: CTL_SW and SYN_SW, plus a series inductor feeding the load to which power at voltage V_o must be supplied. The “load” is generally another electronic circuit requiring power, such as a CPU motherboard, graphics card, or similar. Although the switches shown in prior-art FIG. 1 of the ’190 patent are generic in form, any person skilled in the art would know these switches to be power MOSFETs.

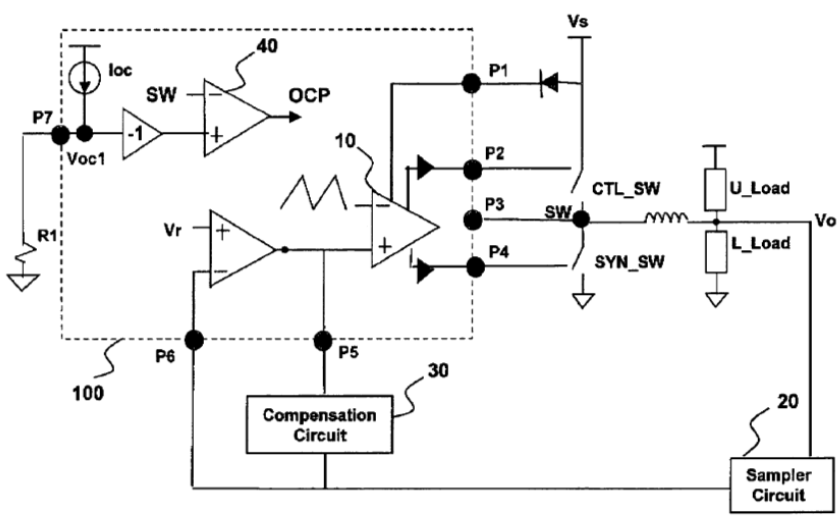


Fig. 1 (Prior Art)

11. The configuration of prior-art **FIG. 1** in which current is fed to the load device by way of a series inductor, is an example of the so-called ‘buck” DC-DC converter. The upper MOSFET (CTL_SW), when in a conducting state (closed circuit), supplies current to the load via the inductor. During this phase of operation, magnetic energy is stored in the inductor for subsequent supply to the load. During the second phase of operation, the upper MOSFET (CTL_SW) is put into its non-conducting state (open circuit) and the lower MOSFET (SYN_SW) is closed. This state allows the current to continue flowing to the load while the energy stored in the inductor during the first phase of operation is supplied to the load. While

the buck regulator is illustrated in some of the embodiments disclosed in the '190 patent, the claims of the patent do not limit the invention to DC-DC converters of the buck type.

12. A person skilled in the art would appreciate that the underlying purpose of the converter, when used as part of a power-supply system, is to keep the output voltage of the power supply constant, regardless of how much power (i.e. current) it must supply to its load. The requirement of constant voltage is typical for equipment powered by the supply. Ideally, such devices would be powered by constant-voltage batteries rather than an electronically derived substitute. Batteries, however, as discussed previously, are often not a viable solution, hence power supplies and DC-to-DC converters are needed.

13. As shown in **Illustration 1**, the load voltage supplied by a PWM converter is kept constant, and equal to a desired, user-determined value, by way of a feedback network. Specifically, the load voltage is sampled, and then fed back to an *error amplifier*. The latter compares the fed-back voltage to a fixed set-point (i.e., reference) voltage, and then produces an output signal that is proportional to the difference between the two inputs. The output of the error amplifier could be a voltage or current, as long as the output is proportional to the difference in inputs. The negative feedback topology of the PWM converter is such that it drives itself into a condition in which the voltage provided to the load is essentially equal to the set- point voltage.

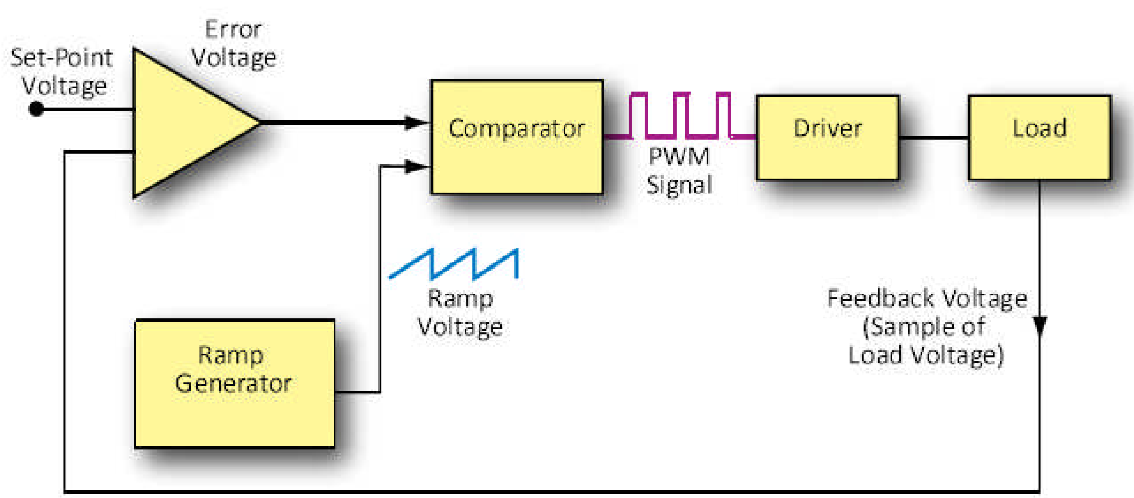


Illustration 1

14. As shown in **Illustration 2**, the converter regulates its output voltage by comparing the output of the error amplifier (the "error signal") to a periodic, rising ramp signal, as shown below. As noted above, this regulation may be realized by comparing voltages or currents. Both the error signal and ramp signal are fed as inputs to a comparator circuit that finds the difference between them, e.g. by subtracting the ramp signal from the error signal.

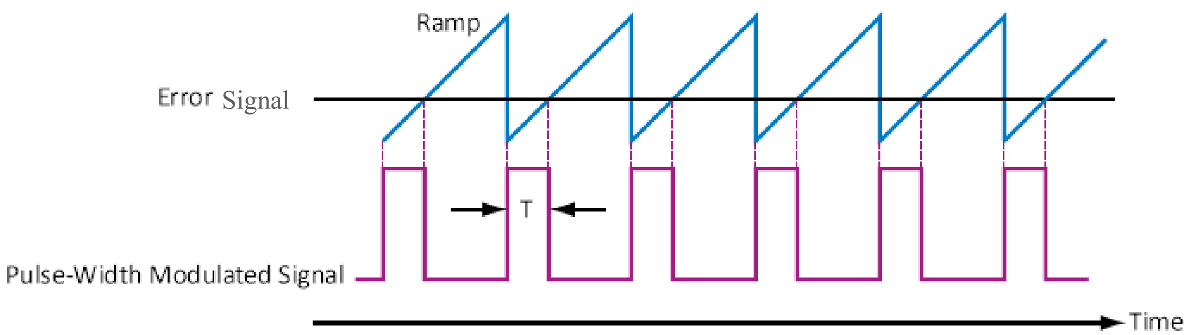


Illustration 2

15. Over the time intervals where the error signal is larger than the instantaneous ramp signal based on the difference between those signals, the comparator output can be high. Conversely, when the error signal is smaller than the ramp signal, the comparator output can be low. The resulting pulse signal coming out of the comparator will thus have a variable width *T* that is determined (i.e., "modulated") by the magnitude of the error signal relative to the peak of the ramp signal. The width *T* of the ensuing pulse waveform determines the time interval over which the upper MOSFET switch in the "totem pole" adds energy to the inductor. A larger *T* will increase the load voltage, whereas a smaller *T* will decrease the load voltage. The net result of this feedback loop is that the converter regulates itself, producing precisely the error signal needed to keep the actual load voltage about equal to the set-point load voltage.

V. EXEMPLARY FEATURES OF THE 190 PATENT

16. The 190 patent, entitled "PWM Circuit and PWM Integrated Circuit For Use in PWM Circuit," was issued to Issac Y. Chen on January 1, 2008, based on an application filed on June 16, 2006. The patent discloses a PWM circuit which may receive a programming signal without requiring an extra pin for this purpose, plus a programming unit to receive the

programming signal for setting or programming a parameter inside the PWM circuit. (**Exhibit B**: 190 Patent at Abstract and 3:53-65).

17. When designing a DC-DC converter to drive a load, the careful practitioner will be mindful of the maximum current that the PWM converter can supply. This limit is generally determined by the MOSFET (MOS) switches comprising the converter's output stage. One key parameter of a MOS device is the maximum current it may safely handle – commonly referred to as its rated current. The rated current for the MOSFETs of a PWM circuit in part dictate the units overcurrent protection (OCP) limit." The OCP limit is determined in part by power dissipation and heat considerations and also by the maximum safe current specified by the manufacturer of the MOSFET itself. (MOSFET switches are often not made the same company that makes the PWM controller.) Exceeding the maximum rated current of a MOSFET can lead to its premature failure, or even to its catastrophic burnout. A large load current might inadvertently cause the MOS current to exceed its rated value. Large currents will also occur due a faulty short circuit downstream of the converter's output. In such situations, a well designed converter will shut down by removing the drive signals to the gates of the MOS switches in the output stage.

18. Referring to FIGS. 1 and 2 of the 190 patent, two conventional ways for overcurrent protection are disclosed. The first conventional (prior-art) way is "to provide a constant current source I_{oc} inside the PWM integrated circuit 100, and a resistor R_1 outside the PWM integrated circuit . . . [b]y means of the constant current source I_{oc} and the resistor R_1, a predetermined voltage is provided at the node Voc1." *Id*. at 1:63-2:2. This predetermined voltage is "compared with the voltage level at the node SW by a comparator 40" that generates an output signal OCP which may be used to trigger overcurrent protection such as the turning off of certain switches. *Id*. at 2:2-10. The second conventional way, which also requires a comparator to trigger over-current protection, "internally generates a reference voltage Voc2, which is input to a comparator 50." The latter generates an output signal OCP to trigger overcurrent protection. *Id*. at 2:12-20. One drawback of these conventional OCP techniques is that they require a separate pin for this purpose. *Id*. at 2:21-24. Another drawback is that it is

not "possible to program the internal circuit inside the PWM integrated circuit unless an additional pin is provided." *Id*. at 2:25-28.

19. As electronic devices, including power supplies, become increasingly smaller, much incentive exists to make IC packages as small as possible by reducing pin count. Pin reduction can be achieved by using some pins for more than one purpose. In this way, total pin count is reduced, leading to a smaller footprint for the packaged IC. In this light, the '190 patent provides a "PWM circuit capable of receiving an external programming signal without an extra pin." *Id*. at 2:37-40. The patent also discloses a "programming unit" to receive the external programming signal that "serves to set/program a parameter such as over-current threshold." *Id*. at 3:12-67.

20. Figures 3, 4 and 6 of the '190 patent disclose examples of PWM integrated circuits evoking reduced pin count while FIGS. 5, 7, and 8 disclose examples of the detailed circuit structure for the programming unit disclosed in the patent. Referring to FIG. 3, reproduced below, this example of the PWM circuit includes a pin P4 that serves two purposes. Firstly, pin P4 is used for controlling the synchronous switch SYN_SW in a normal mode. Secondly, the pin is used for setting/programming a parameter while in a programming mode. *Id*. at 3:12-23; 3:53-19. The programming mode to set the OCP would typically be evoked during the power-up phase of the PWM circuit after its power source has been turned on but before it actually begins producing power -- a necessary and essential function for the circuit to operate properly.

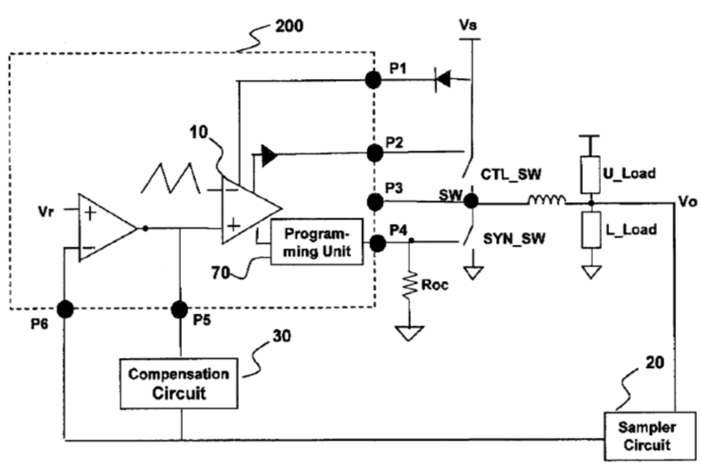


Fig. 3

21. As show in FIG. 3, the PWM integrated circuit 200 is contained within the dotted line. The other components shown are external to the integrated circuit. The PWM comparator 10, which accepts the error signal and ramp signals as inputs, drives pins P2 and P4 in the normal mode, thereby servicing the gates of the upper and lower MOSFET switches (CTL_SW and SYN_SW).

22. Pin P4 indeed serves the dual purpose described in the patent. That is, the normal mode allows the output from the PWM comparator to pass to the SYN_SW (lower) MOS switch. In the programming mode, the PWM comparator output does not appear on pin P4. Rather, the pin senses a programming signal derived from the voltage across resistor R_{OC} via a small DC test current sent through R_{OC}. The voltage thereby developed across R_{OC}, as determined by Ohm's law (voltage = current × resistance) is received by the programming unit and stored so as to set a parameter to program the over-current threshold level. The latter is compared to the total load current in normal mode. If the load current exceeds the overcurrent threshold level, the circuit will turn off its drive to the output switches to prevent damage from an excessive current condition. *Id*. at 3:53-4:67.

23. While the lower switch pin P4 is used to receive a signal into the programming unit in FIG. 3, it is also possible to use the upper pin P2 for this purpose, as in FIG. 4. Alternatively, the signal can be received between P2 and P4, as shown in FIG. 6. These alternative examples provide for flexibility in implementation, but do not alter the scope of the patent, which is to reduce overall pin count of the PWM integrated circuit. FIG. 5, reproduced below, shows one example of the detailed structure for the programming unit.

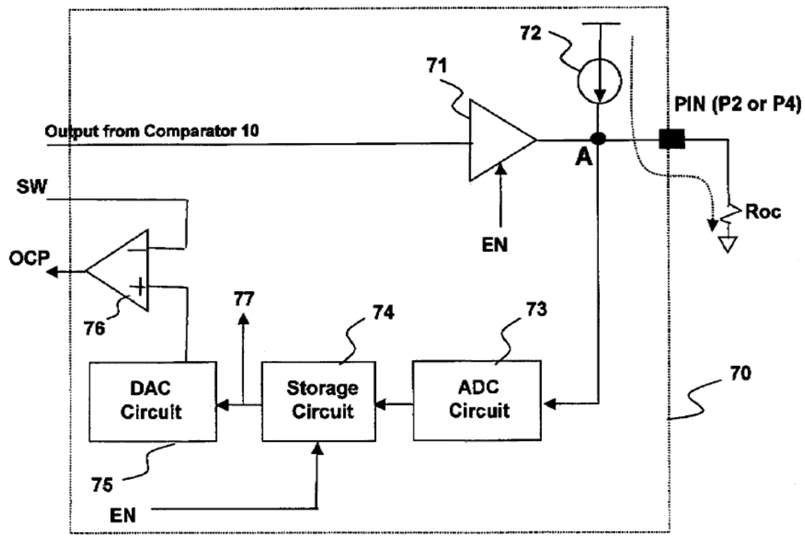


Fig. 5

24. As shown above, when the controller is in programming mode, the current source 72 sends current through R_{OC}. The voltage developed across R_{OC} is read by the analog-to-digital (A/D or ADC) converter circuit 73, which transforms the analog voltage signal at P4 into a digital signal. The latter is a collection of binary ones "1" and zeros "0" that comprise a digital representation of the voltage developed across R_{OC}. The digital information is stored in storage circuit 74 to set a parameter such as the over-current threshold level OCP. The digital-to-analog converter (D/A or DAC) circuit 75 transforms the digital version of the analog signal derived from *Roc* back into an analog signal that can be compared, via comparator 76, with the signal SW representing the load current. When the latter exceeds the OCP threshold, the comparator 76 generates an OCP ("overcurrent protection") control signal to remove the drive from the output switches CTL_SW and SYN_SW. *Id*. at 4:19-6:3.

25. An additional feature of the programming unit disclosed in the patent is its use of tri-state drivers in FIGS. 5, 7, and 8 (71, 81U, 81L, 91U, and 91L). These drivers receive outputs from the comparator circuit 10 that receives the programming signal. In the digital world, an output will be either "high" (equal to 1), essentially connected to the supply voltage powering the chip, or "low" (equal to 0), and essentially connected to ground. If an output is of the tri-state type, however, it will have a third state in which the output terminal is connected to

neither the supply voltage nor ground. Rather, it is left electrically "floating." This feature allows something else connected to the same terminal to use the latter as an input, rather than an output, as shown in FIGS. 5, 7, and 8. *Id*. at 4:19-6:46.

VI. CLAIMS AT ISSUE

26. In this lawsuit, I understand that Richtek has asserted infringement over claims 1-11 and 26-27 of the 190 patent against the accused products. I also understand that the Examiner has issued a NOA rejecting claims 1-11 and 26-27 of the 190 based on two Intersil datasheets. Claims 1, 26, and 27 are independent claims, and claims 2-11 depend from claim 1. Claim 1 is representative and reproduced below:

> 1. A pulse width modulation circuit comprising:
> a first and a second switch electrically connected with each other through a node between them, said node being capable of providing a voltage signal;
> a PWM integrated circuit, including
> (a) a plurality of pins including a first pin for controlling said first switch, a second pin for controlling said second switch, and a third pin for receiving said voltage signal from said node; and
> (b) a programming unit electrically connected with one of said first pin and second pin, for receiving a programming signal to program a parameter of said pulse width modulation integrated circuit; and
> a parameter setting circuit electrically connected with said one of said first pin and second pin.

(**Exhibit B**: 190 Patent at 7:2-16).

27. I believe that each the terms in claims 1-11 and 26-27 of the 190 patent has a plain and well understood ordinary meaning to those skilled in the art in view of the 190 patent, its file history, cited references ordinary, and literature in the related art at the time of the invention of the 190 patent. I have analyzed the references cited by the Examiner in view of the ordinary meaning that would be given to these terms as understood by one of ordinary skill art. It is my opinions that these claims are valid over the references relied upon by the Examiner in the NOA.

VII. LEVEL OF ORDINARY SKILL

28. I understand that claims are understood from the perspective of one of ordinary skill in the relevant art. Based on my experience and expertise, plus my review of the 190 patent and related information, it is my opinion that the relevant art is switching power supplies such as DC-DC converters using PWM control techniques. It is also my opinion that, at the time of filing of the 190 patent, one of ordinary skill would have had an understanding of switching power supplies such as DC-DC converters and PWM control techniques and possess at least: (1) a B.S. degree in Electrical Engineering and 2 to 4 years of relevant work experience in the area of switching power supplies and PWM techniques; or (2) a M.S. degree in Electrical Engineering studying switching power supplies and PWM control techniques with at least 1 to 2 years of relevant work experience. Based on this level of ordinary skill, I provide my analysis of validity related to claims 1-11 and 26-26 of the 190 patent.

VIII. PROOF NEEDED TO SHOW INVALIDITY

29. I understand that a United States Patent that is examined and issued is presumed valid. I also understand that showing a United States Patent to be invalid requires a high burden of proof such as "clear and convincing evidence." I have reviewed the NOA by the Examiner and the two Intersil Datasheets (**Exhibits D** and **E**) in view of claims 1-11 and 26-27 of the 190 patent. It is my opinion that these two references fail to meet the high burden of proof to show invalidity and it is my opinion that claims 1-11 and 26-27 are valid over them.

A. Requirements to Prove Anticipation

30. I understand that a patent claim may be declared invalid due to anticipation if the elements of the patent claim are disclosed in a prior art reference. I am informed that this standard is set forth in 35 U.S.C. §§ 102(a), (b), and (e)(2), which are reproduced in pertinent part below:

> 35 U.S.C. § 102 - A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent, or
>
> (b) the invention was patented or described in a printed

> publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States, or
>
> (e) the invention was described in . . . (2) a patent granted on an application for patent by another filed in the United States before invention by the applicant for patent . . .

31. I understand that anticipation under the patent statute 35 U.S.C. §§ 102 (a), (b), and (e) involves a comparison of construed claims to the alleged prior art. In order to anticipate a patent claim, I am informed that a single prior art reference must disclose each and every element of the claimed invention, either expressly or inherently.

32. I further understand that such a reference must be accessible to the public. Thus, I understand that documents maintained in confidence or not publicly available cannot be considered prior art under this statute. I further understand that in order for an invention to be "known" or "used by others in this country" the invention's knowledge or use must have been accessible to the public such that it places the claimed invention in the possession of the public.

33. I also understand that a prior art reference must be enabling. That is, it must teach one of ordinary skill in the art how to make or carry out the claimed invention without undue experimentation and must place the claimed subject matter in the possession of the public. I am informed that whether claims are sufficiently enabled by a disclosure in a specification is determined as of the date that the patent application was first filed. I am further informed that an enablement determination is made retrospectively, *i.e.*, by looking back to the filing date of the patent application and determining whether undue experimentation would have been required to make and use the claimed invention at that time. I am further informed that whether the requisite amount of experimentation is "undue" may include consideration of: (1) the quantity of experimentation necessary, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims.

34. I also understand that under 35 U.S.C. § 102(b) a claim is anticipated if a printed publication or product practicing each and every limitation of the claim was in public use,

offered for sale, or on sale in the U.S. more than one year prior to the date of the application for the patent. The filing date for the 190 patent in the United States is June 16, 2006. In order to anticipate the 190 patent under 102(b), the critical date is June 16, 2005.

B. Requirements to Prove Obviousness

35. I understand that a patent claim may be declared invalid if the elements of the patent claim are obvious in view of the prior art. I am informed that this standard is set forth in the patent statute 35 U.S.C. § 103(a), which has been reproduced in pertinent part below:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains.

36. I also understand that a patent claim composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. It is important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way as claimed an issued by the United States Patent Office. I also note that most if not all inventions rely on building blocks in which each building block may have been known. Thus, claimed inventions and their new discoveries almost out of necessity will be combinations of what, in some sense, is already known. I understand that, in approaching the question of obviousness, one should be aware of the potential distortion of hindsight and should guard against reading the teachings of the patented invention itself into the prior art based on hindsight. I understand doing the later to be improper to do in making an obvious and invalidity determination. I also understand that secondary considerations such as commercial success, failure of others, recognition by others, long felt but unresolved needs, and copying can be strong and compelling evidence that an invention is not obvious.

37. In this Declaration, based on the level of one of ordinary skill noted above, I have analyzed the 190 patent and the NOA provided by the Examiner and the two Intersil

Datasheets with these principles in mind in concluding that claims 1-11 and 26-27 of the 190 patent are valid.

IX. VALIDITY ANALYSIS

38. In the December 17, 2010 NOA (**Exhibit C**), the Examiner relied on two Intersil Datasheets which were provided with the NOA: (1) Intersil ISL6545, ISL6545A Datasheet **April 29, 2010** FN6305 for a "5V or 12V Single Synchronous Buck Pulse-Width Modulation PWM Controller" ("ISL6545 Datasheet"); (2) Intersil ISL6520 Datasheet March 2003 FN9009.2 for a "Single Synchronous Buck Pulse-Width Modulation PWM Controller" ("ISL6520 Datasheet"). I have reviewed the Examiner's NOA and the ISL6545 Datasheet and ISL6520 Datasheet (collectively "ISL65xx Datasheets") and it is my opinion that claims 1-11 and 26-27 of the 190 patent are valid over them.

A. The ISL6545 Datasheet and ISL6520 Datasheets Are Not Anticipatory Prior Art

39. In the NOA, the Examiner rejected claims 1-7, 9, 26, and 27 of the 190 patent as allegedly anticipated by the ISL6545 Datasheet. Specifically, the Examiner cited the ISL6545 Datasheet as allegedly being published in October 2005:

> ISL6545 bears the date of **October 10th, 2005**, which is prior art to the critical date of the '190 patent... ISL6545 DS is material to the patentability of the '190 patent.

Exhibit C at 2 (emphasis added). But, the ISL6545 Datasheet provided by the Examiner with the NOA is dated **April 29, 2010** and therefore cannot constitute anticipatory prior art because the 190 patent was filed on **June 16, 2006**.

1. The ISL6545 Datasheet is Not a Printed Publication That is Publicly Available and Cannot Be Considered Prior Art

40. I performed extensive searching looking for an ISL6545 Datasheet dated October 2005 and could not find it. Specifically, I conducted Internet searches via Google and comprehensive Internet searching via *waybackmachine.org*, probing Intersil's own website, and full-text searches using the library journal and publication engineering database services *ieeexplore* and *Inspec*. The earliest datasheet that I have found for the ISL6545 chip was dated

November 15, 2006 not October 2005 (**Exhibit F**). This date also coincides with the date of a press release issued by Intersil in November 22, 2006 announcing the 6545 chip to the market. (**Exhibit G**). I also note that revised data sheets for the ISL6545 were published in July 2007 and April 2010, both well after the June 16, 2006 filing date of the 190 patent.

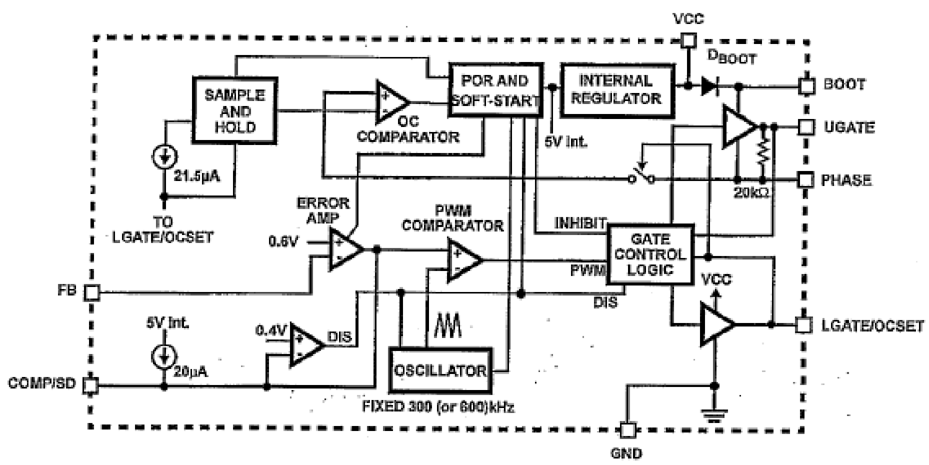
41. This is also consistent with testimony I reviewed in a related ITC Investigation No. 337-TA-698 ("ITC Investigation") of an Intersil employee. Because I cannot disclose that information in the ITC Investigation, I nevertheless formed an understanding that the ISL6545 Datasheet supposedly dated October 2005 was considered "Confidential," and it is my understanding was not publicly available or freely distributed to the public. This possibly explains why the Examiner could not provide the October 2005 ISL6545 Datasheet. Nevertheless, it is my opinion that an October 2005 ISL6545 Datasheet is not publicly available and cannot be considered prior art because it is not a publication that is publicly available.

2. The ISL6545 and ISL6520 Datasheets Are Non-Enabling

42. In my opinion, even if the ISL6545 Datasheet was published in October 2005, the ISL65xx Datasheets would still not constitute anticipatory prior art because they are non-enabling. They do not provide an enabling disclosure for one of ordinary skill to make and practice claims 1-11 and 26-27 of the 190 patent. In other words, the ISL65xx Datasheets do not put the claimed inventions in the possession of the public through an enabling disclosure.

43. For example, the Examiner relies on the internal block diagram (shown below) on page 3 of the ISL6545 Datasheet allegedly showing components of claims 1-11 and 26-27 of the 190 patent (the block diagram in the ISL6520 Datasheet has even less components.):

Block Diagram



44. I note in the above block diagram describe only top-level functionality. In my opinion, such block diagrams and sparse corresponding text in the datasheets do not teach or enable one of ordinary skill to make and use the integrated circuits described by the datasheets. There is nothing in the ISL65xx Datasheets identifying any entities as a programming unit, nor can one of ordinary skill find a programming unit, analog-to-digital (A/D) converter, digital-to-analog (D/A) converter, storage unit, tri-state driver, etc. as required in the claims of the 190 patent. These components are explicitly required by in the claims of the 190 patent. In light of the vagueness in the ISL65xx Datasheets, I do not believe that they provide sufficient description to enable a person of skill to make and practice claims 1-11 and 26-27 of the 190 patent.

45. Furthermore, the ISL6520 datasheet refers to the concept of programming only with respect to choosing the parameter-setting resistor:

> A resistor (ROCSET) programs the over-current trip level (see Typical Application diagram). (*see* ISL6520 and ISL6545 datasheets, pgs. 4 and 7, respectively.)

46. No mention is made of the architecture or structure inside the chip that does the programming. For example, the ISL6545 Datasheet includes one additional reference to the concept of programming:

> The output voltage can be programmed to any level between the 0.6 V internal reference, up to the V_{IN} supply.

> The ISL6545 can run at near 100% duty cycle at zero load, but the $r_{DS(ON)}$ of the upper MOSFET will effectively limit it to something less as the load current increases. In addition, the OCP (if enabled) will also limit the maximum effective duty cycle. (ISL6545 datasheet, page 8)

47. This instruction pertains to the setting of the converter's output voltage, however, and is unrelated to setting the overcurrent protection level via R_{OCSET}. Hence, it is totally unrelated to the programming-unit concept as disclosed in the 190 patent. The ISL65xx Datasheets indicate that the voltage sampled across the parameter-setting resistor R_{OCSET} can be held indefinitely, but no explanation is given as to how this feat is accomplished. The 190 patent is explicit in this regard, requiring A/D and D/A converters and memory circuitry to store the parameter value (e.g., voltage) measured across R_{OCSET}.

48. Unlike the 190 patent, the ISL65xx Datasheets are vague and provide no detail as to how the programming is to be performed. The 190 patent, however, provides more than sufficient detail to enable one of ordinary skill to practice and use the claimed invention and, in particular, how to implement and practice the claimed "programming unit" and other claimed components. For example, the patent describes three different examples of a programming unit in FIGS. 5, 7, and 8 and explains in detail and at length how to program a parameter for the PWM integrated circuit at least on 4:20-6:4; 6:33-67 (**Exhibit B**: 190 Patent at RTK00000012-13). Such detail is not provided in the ISL65xx Datasheets. Thus, in light of the vague and insufficient detail in the ISL65xx Datasheets, it is my opinion that ISL65xx Datasheets do not enable a person of ordinary skill in the art to make and practice claims 1-11 and 26-27 of the 190 patent.

3. The ISL6545 Datasheet and ISL6520 Datasheet Do Not Disclose All the Elements of Claims 1-11 and 26-27

49. I have compared claims 1-11 and 26-27 of the 190 patent with the ISL65xx Datasheets provided by the Examiner in the NOA and do not find each and every element of the claims in the datasheets. It is my understanding if there is one missing element in the references it cannot anticipate the claims. Because I have found missing claim elements in the ISL65xx Datasheets, it is my opinion claims 1-11 and 26-27 are valid over the ISL65xx Datasheets.

(a) The Programming Unit in Claims 1-11 is Missing

50. In the NOA, the Examiner identified the "SAMPLE AND HOLD" and "POR AND SOFTSTART" together with the 20uA current source and OC comparator and two driver gates in the ISL6545 Datasheet as the claimed "programming unit" in claims 1, 26, and 27. **Exhibit C**, NOA at 4-5. In claim 1, however, the "programming unit" is recited as:

> (b) a programming unit electrically **connected with one of said first pin and second pin**, for receiving a programming signal to program a parameter of said pulse width modulation integrated circuit; and

(**Exhibit B**: 190 Patent at 7:11-14).

51. In my opinion, one of ordinary skill would not view these collection components as the claimed "programming unit." The ISL6545 Datasheet does not describe any of these components as a "programming unit." I believe that Examiner erred in his analysis. Specifically, the Examiner has not described how this collection of components, if considered as a "programming unit" can be "connected to **one** of said first pin and second pin." In the NOA, the Examiner alleged:

> ISL6545 DS discloses a programming unit electrically connected with one of said first and second pin for receiving a programming signal to program a parameter set pulse width modulation.

(**Exhibit C**, NOA, at 4).

52. The functional circuit blocks indentified by the Examiner as the "programming unit" in the block diagram of the ISL6545 Datasheet show two driver gates (triangle shaped symbol) connected to respective UGATE and LGATE pins identified by the Examiner as the claimed first and second pins. If the driver gates are part of the programming unit, such a programming unit would not meet the limitations of the claims because it is not *one* pin (but both pins) of the MOSFET gates. In other words, the programming unit identified by the Examiner is not connected to one "**one** of said first pin and second pin" required in claims 1-11.

53. The plain meaning of the claim language in claims 1-11 is that the programming unit must be connected to **one** of the two pins. Examples of this feature are shown below in FIGS. 3 and 4 below:

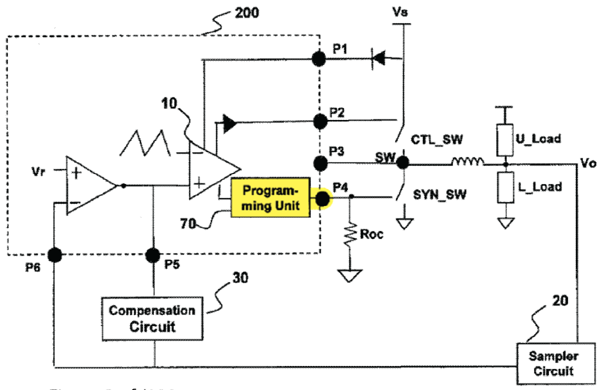


Figure 3 of ’190 patent

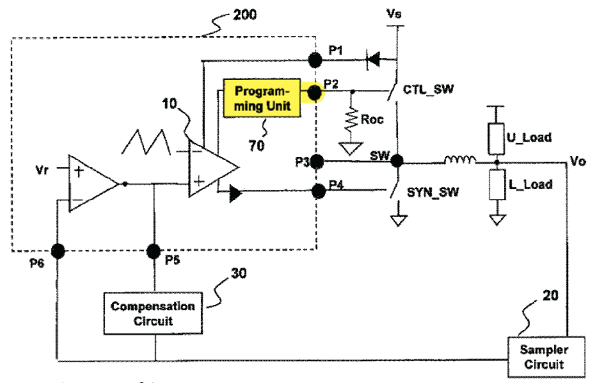


Figure 4 of ’190 patent

54. The 190 patent is explicit in disclosing a programming unit that connects to the same pin as the parameter setting circuit (*e.g.*, to pin P_4, one of the MOSFET gate connections, in FIG. 3 of the 190 patent). The 190 patent further describes such a feature and its functionality for the programming unit:

> In the programming mode, the programming unit 70 serves to set/program a parameter, such as an over-current threshold or other programmable parameters, in the integrated circuit 200. After the setting/programming is done, the programming unit 70 may be switched to the normal operation mode wherein **the programming unit 70 becomes a normal driver gate transmitting the output of the comparator 10 to the synchronous switch SYN_SW**.

Id. at 3:63-66.

55. Thus, in addition to its connection to a MOSFET gate pin, the programming unit must perform the task of driving the gate to which it is connected. There is nothing in the ISL65xx Datasheets that show a programming unit driving one of the MOSFET gates.

56. I note that there is no mention in the ISL6545 Datasheet of the architecture or structure inside the chip that does the programming. The ISL6545 datasheet includes one additional reference to the concept of programming:

> The output voltage can be programmed to any level between the 0.6 V internal reference, up to the V_{IN} supply. The ISL6545 can run at near 100% duty cycle at zero load, but the $r_{DS(ON)}$ of the upper MOSFET will effectively limit it to something less as the load current increases. In addition, the OCP (if enabled) will also limit the maximum effective duty cycle.

(**Exhibit D**, ISL6545 Datasheet, at 8).This instruction, however, pertains to the setting of the

converter's output voltage, and has nothing to do with the setting of the overcurrent-protection level via R_{OCSET}. Hence this instance of the word "programmed" is totally unrelated to the programming-unit concept as disclosed in the 190 patent.

57. The ISL65xx Datasheets also indicate that the voltage sampled across the parameter-setting resistor R_{OCSET} can be held indefinitely, but no explanation is given as to how this feat is accomplished. The 190 patent is explicit in this regard, requiring A/D and D/A converters and memory circuitry to store the parameter value (*e.g.*, voltage) measured across R_{OCSET}. Unlike the 190 patent, the Intersil ISL65xx Datasheets are too vague and provide no detail as to how the programming is to be performed.

58. Yet, the Examiner cites the power on reset (POR) function as evidence that the ISL65xx Datasheets contain a programming unit. The POR circuit, however, has nothing to do with programming. Rather, it is a timing sequencer that initiates and monitors various phases of startup; it does no programming, but instead serves to mark the point in time, for example, when the reading of the parameter setting circuit occurs. It thus has nothing to do with the claimed programming unit of the 190 patent. Accordingly, it is my opinion that one of ordinary skill would not find the programming unit in the ISL65xx Datasheets and, therefore, claim 1 of the 190 patent is valid over the ISL6545 Datasheet. Because the dependent claims 2-11 require the missing programming unit, those dependent claims are valid over the ISL65xx Datasheets.

(b) The Parameter Setting Circuit is Missing in Claims 1-11

59. Claims 1-11 require "a *parameter setting circuit* electrically connected with said one of the first pin and second pin." This requires the setting circuit to be connected to the one that the programming unit is required to be connected to. The first and second pins refer to the antecedent connections to the terminals that control the "first" and "second" switches. The claim element requires that the parameter-setting circuit be connected to one of the two pins that drive the MOSFET gates, *i.e.*, the gates of the MOSFETs used in the power converter. This claim feature is exemplified in FIGS. 3 and 4 the 190 patent, where the resistor R_{oc} is connected either to pin P_4 or to pin P_2, respectively. The ISL6520 datasheet illustrates neither such scenario. Its parameter-setting resistor R_{OCSET} is connected to the chip's COMP pin; the latter

connects internally to the output of the error amplifier, but not to any MOSFET gate. Thus this core feature of the patent, namely that R_{OCSET} be connected to the gate of the upper MOSFET or lower MOSFET, is not present on the ISL6520 datasheet. The ISL6520 datasheet describes the connection point for R_{OCSET} (COMP/OCSET) as follows:

> This is a multiplexed pin. During a short period of time following power-on-reset, this pin is used to determine the over-current threshold of the converter. Connect a resistor from this pin to the drain of the upper MOSFET (V_{CC}).

Exhibit E, ISL6520 Datasheet, at 4.

60. The voltage bus V_{CC}, of course, refers to the power supply used to power the chip, and not to either of the pins that drive MOSFET gates. In contrast to the ISL6520 chip, the ISL6545 chip uses its COMP/SD pin in an alternative fashion:

> This is a multiplexed pin. During soft start and normal converter operation, this pin represents the output of the error amplifier. Use COMP/ST in combination with the FB pin to compensate the voltage-control feedback loop of the converter. Pulling COMP/ST low will shut down (disable) the controller, which causes the oscillator to stop, the LGATE and UGATE outputs to be held low, and the soft start circuitry to rearm.

Exhibit D, ISL6545 Datasheet, at 5.

61. Thus, while the non-prior-art ISL6545 does disclose connecting a parameter-setting resistor to one of the MOSFET gates, the prior-art ISL6520 does not. But, the ISL6545 does not teach that a programming unit is also solely connected to the gate the resistor is connected to. Without this teaching, the parameter setting circuit element is also not met in claims 1-11.

(c) Elements in Claims 2-11 and 26-27 Are Also Missing

62. In the NOA, the Examiner did not provide any chart or analysis for dependent claims 2-11 regarding the ISL6545 Datasheet. I have compared the dependent claims 2-11 with the ISL6545 Datasheet and, in addition to the missing programming unit, it is my opinion the datasheet fails to disclose all of the elements in dependent claims 2-11 because they are simply not taught and the Examiner has not pointed to anything in the datasheet for those features.

63. For example, claim 2 requires that the programming unit include "a constant current source electrically connected with said one of said first pin and second pin." The ISL6545 Datasheet shows a current source, but the latter is connected to the COMP pin, not to a MOSFET gate pin. Claim 3 requires that the programming unit "transmit said output of said comparator to said one of said first pin and second pin, while in a programming mode, said programming unit receives said programming signal." In other words, the two states of the programming unit are associated with the driving of the MOSFET gate. This feature is not described in any way that would be enabling in either of the ISL65xx Datasheets. Rather, the collection of blocks identified by the Examiner as supposedly constituting the "programming unit" simply show that some digital control is occurring within both chips. In fact, the block diagrams shown in ISL65xx Datasheets more closely resemble those found on FIG. 2 of the 190 patent, which illustrates prior art to the '190 patent.

64. Claim 4 requires that the programming unit "switch between said normal operation mode and said programming mode according to an enable signal" not disclosed in the ISL65xx Datasheets. FIG. 5 of the 190 patent explicitly shows how the programming unit either passes or does not pass the comparator output by way of an enable signal. A description of such a feature is absent on the ISL6545A datasheet. Claim 5 further requires that the programming unit have a tri-state driver. The Examiner suggests that the ISL6545 datasheet contains a tri-state driver (page 11), but the term "tri-state driver" or any close derivative of this term appears nowhere on either Intersil datasheet. Moreover, there is nothing at all on either datasheet that would even suggest that a tri-state driver is present.

65. Claim 8 requires that the analog-to-digital converter be connected directly to one of the MOSFET gate pins, as illustrated, for example, in FIG. 5 of the 190 patent. Neither Intersil datasheet shows an A/D converter connected to the pin of a MOSFET. In fact, the datasheets simply mention that the voltage across R_{OCSET} is sampled and held by a sample-and-hold circuit. This explanation falls far short of specifying an A/D converter as part of this sampling operation. On the issue of signal conversion, the ISL6545 datasheet does mention (twice) the concept of digital-to-analog conversion, mentioning "a counter and DAC

combination." This description is a vague reference to one method of producing an analog-to-digital converter (e.g., from a DAC and a counter), but nowhere does the datasheet discuss this configuration in any detail or explain its operation. Such vague teachings apply equally to the rest of dependent claims 9-11.

66. Claims 26 and 27 require the presence of a two-output comparator, a programming unit that changes between two modes, and a tri-state driver. The programming unit must have the functionality of programming. There is nothing in the ISL65xx Datasheets show a programming unit, and the two modes required of the claims are not described. Similarly, the term "tri-state driver" or closely related term appear nowhere to be found in the ISL65xx Datasheets. Simply stated, there is nothing at all in these datasheets that indicates that a tri-state driver is present. Accordingly, it is my opinion that claims 2-11 and 26 and 27 are valid over the ISL65xx Datasheets.

B. The ISL6545 and ISL6520 Datasheets Do Not Render the 190 Patent Obvious

67. The Examiner rejects claims 8, 10, and 11 as obvious in view of the ISL6545 Datasheet in combination with the ISL6520 Datasheet, conceding that the ISL6545 Datasheet is deficient in its disclosure. However, as noted above, there are numerous missing elements in both the ISL6545 and ISL6520 Datasheets that no one skilled in the art considering these references, alone or in combination, would find claims 1-11 and 26-27 of the patent as obvious. Thus, it is my opinion that claims 1-11 and 26-27 of the 190 patent are valid over the ISL65xx Datasheets cited by the Examiner.

X. <u>CONCLUSION</u>

68. Based on the analysis and review of the NOA and two Intersil datasheets, it is my opinion that the ISL6545 Datasheet and the ISL6520 Datasheet to not provide clear and convincing evidence to show that any of the asserted claims 1-11 and 26-27 of the 190 patent are invalid for anticipation or obviousness. I therefore conclude that claims 1-11 and 26-27 of the 190 patent are valid and as I have explained in this Declaration.

I declare under penalty of perjury under the laws of the United States of America that

the foregoing is true and correct.

Executed on January 20, 2011 in Boston, Massachusetts.

/s/ Mark Horenstein, Ph.D.
Mark Horenstein, Ph.D.

FILER'S ATTESTATION

Pursuant to General Order No. 45, Section X (B) regarding signatures, I, S. H. Michael Kim, attest that concurrence in the filing of this document has been obtained.

/s/ S.H. Michael Kim
S.H. Michael Kim

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